What is claimed is:

CLAIMS

1. A method for fabricating a nanoscopic transistor, comprising the steps of:

a) providing a semiconductor substrate;

b) forming a thin oxide layer on the semiconductor substrate;

c) applying a first layer of resist;

d) patterning the first layer of resist using imprint lithography to form a first pattern aligned along a first direction;

e) applying a first ion-masking material over the first pattern, and selectively lifting off the first ion-masking material to leave a first ion mask defined by the first pattern, the first ion mask optionally being suitable to form a gate;

f) forming first doped regions in the semiconductor substrate by implanting a suitable first dopant selectively in accordance with the first ion mask;

g) applying a second layer of resist and patterning the second layer of resist using imprint lithography to form a second pattern aligned along a second direction;

h) applying a second ion-masking material over the second pattern, and selectively lifting off the second ion-masking material to leave a second ion mask defined by the second pattern; and

i) forming second doped regions in the semiconductor substrate by implanting a suitable second dopant selectively in accordance with the second ion mask.

2. The method of claim 1, wherein the second direction is substantially orthogonal to the first direction.

3. The method of claim 1, wherein the first ion mask is left in place after the step f) of forming source and drain regions, whereby the first ion mask is suitably disposed to serve as a gate electrode.

4. The method of claim 1, further comprising the step of:

j) depositing a conductive material before the step e) of applying a first ion-masking material, whereby the conductive material is patterned to serve as a gate electrode.

5. The method of claim 4, further comprising the step of:

k) removing the first ion mask after the step f) of forming source and drain regions.

6. The method of claim 1, further comprising the step of:

l) removing the first ion mask after the step f) of forming source and drain regions.

7. The method of claim 1, wherein the semiconductor substrate is P- and the first doped regions form P++ regions suitable for isolation regions.

8. The method of claim 1, wherein the semiconductor substrate is P- and the second doped regions form N+ regions suitable for second source and drain regions.

9. The method of claim 1, wherein the smallest dimension of the first pattern is less than about one micrometer.

10. The method of claim 1, wherein the smallest dimension of the second pattern is less than about one micrometer.

11. The method of claim 1, wherein the smallest dimension of the first pattern and the smallest dimension of the second pattern are both less than about one micrometer.

12. The method of claim 1, wherein the smallest dimension of the first doped regions is less than about one micrometer.

13. The method of claim 1, wherein the smallest dimension of the second doped regions is less than about one micrometer.

14. The method of claim 1, wherein the smallest dimension of the first pattern, the smallest dimension of the second pattern, the smallest dimension of the first doped regions, and the smallest dimension of the second doped regions are all less than about one micrometer.

15. The method of claim 1, further comprising the step of:

forming a second gate insulated from the gate electrode and from the semiconductor substrate, the second gate being disposed between the gate electrode and the semiconductor substrate.

16. The method of claim 1, wherein the steps are performed in the order recited.

17. A method for fabricating an array of nanoscopic transistors, comprising the steps of claim 1, wherein the first and second patterns define a multiplicity of transistors disposed in an array.

18. An integrated circuit fabricated by the method of claim 17.

19. An electronic device fabricated by the method of claim 17.

20. The method of claim 17, wherein the first and second patterns further define a plurality of conductive interconnections, the method further comprising the step of:

selectively severing the conductive interconnections to selectively subdivide the array of nanoscopic transistors into cells.

21. An array of nanoscopic transistors comprising:

a) a semiconductor substrate of a predetermined conductivity type and having a major surface;

b) a multiplicity of first nanoscopic transistors comprising first doped regions of a second predetermined conductivity type, the first doped regions being disposed in the major surface of the semiconductor substrate and being arranged in parallel rows at least partially aligned along a first direction, the first doped regions being pairwise spaced apart by a first distance less than about one micrometer, the first distance defining lengths of first channels, and further comprising a multiplicity of first gate electrodes, each first gate electrode being aligned over one of the first channels;

c) a multiplicity of second nanoscopic transistors comprising second doped regions of a third predetermined conductivity type, the second doped regions being disposed in the major surface of the semiconductor substrate and being arranged in parallel columns at least partially aligned along a second direction, the second doped regions being pairwise spaced apart by a second distance less than about one micrometer, the second distance defining lengths of second channels, and further comprising a multiplicity of second gate electrodes, each second gate electrode being aligned over one of the second channels; and

d) conductive interconnections aligned parallel to the first and second directions, the conductive interconnections selectively interconnecting the first and second nanoscopic transistors.

22. The array of claim 21, wherein the first and second directions are substantially orthogonal.

23. The array of claim 21, wherein the conductive interconnections comprise conductive segments and the conductive interconnections are programmable by selective severing of conductive segments.

24. An integrated circuit comprising:

a) an array of nanoscopic transistors formed in semiconductive means of a predetermined conductivity type for carrying the nanoscopic transistors;

b) first conductive means for interconnecting the nanoscopic transistors, the first conductive means for interconnecting being at least partially aligned along a first direction;

c) second conductive means for interconnecting the nanoscopic transistors, the second conductive means for interconnecting being at least partially aligned along a second direction; and

d) conductive interconnections aligned parallel to the first and second directions, the conductive interconnections selectively interconnecting the first and second nanoscopic transistors.